LVDS (EIA644) – USB2.0 Converter Unit

ARTUST-0405A-LV (no memory)

Safety Concern:

- *Safety instructions should be read before the product is operated.
- *All operating and use instructions should be followed.

Warning and Caution:

Warning	Ignoring this Warning mark and operating this product incorrectly may
	lead to serious injury or death
Caution 🚹	Ignoring this Caution mark and operating this product incorrectly may lead to injury or damage to the product.

MWarning

To reduce the risk of fire or shock hazard, do not expose this equipment to rain or moisture

Do NOT use this equipment in the vicinity of flammable or explosive gas

Do NOT leave this equipment within the reach of infants or children

Do NOT store this equipment in humid or dusty places. This may cause fire or electric shock

ACaution

To reduce the risk of electric shock, do NOT remove cover

Never attempt to disassemble this equipment. It contains high-voltage circuitry that may cause electric shock and injury.

Do NOT operate the equipment with wet hands as you may get an electric shock Do NOT store the equipment in any place exposed to excessive heat. This may weaken the parts or cause a fire

1. Description

LVDS-USB2.0 converter unit enables you to transfer parallel output signal from LVDS digital camera output (EIA644, etc.) into your PC via USB2.0 interface.

2. Main Features

*High-speed transfer of up to 35M byte/s via USB2 (Actual value obtained by PC's with ICH4 host controller. Jan 2003). (Theoretical value=60Mbyte/s)

*IO interface that can be externally controlled by API is also available LTTL: 8 bit (output), LVDS: 5 bit (option)

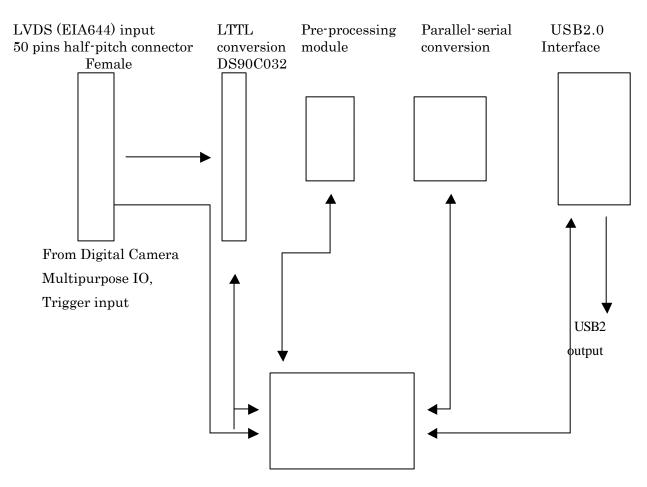
*Size of capturing images can be altered from software conrol

* The size of outer shape (PCB) is $150 \text{mm} \times 100 \text{mm} \times 15 \text{mm}$

*Power consumption: 5V, below 0.5A

*Format of driver: WDM format, compatible with Windows2000/XP

3. Block Diagram: ARTUST 0405A-LV LVDS(EIA644) input LTTL conversion



Timing controller FPGA

4. Input Pin Assignment

Connector: DX10A-50S (Hirose) Cable side: DX30-50P (Hirose)
Input I C : DS90LV032TM Cover: DX-50-CV1 (Hirose)

PIN		PIN	SIGNAL	PIN	SINGLE	PIN	SINGLE
	SIGNAL						
1	CTL0(+)	14	Cam_IO5	27	D4(+)	40	D10(-)
2	CTL0(-)	15	Cam_IO6	28	D4(-)	41	D11(+)
3	CTL1(+)	16	Cam_IO7	29	D5(+)	42	D11(-)
4	CTL1(-)	17	GND	30	D5(-)	43	vd(+)
5	CTL2(+)	18	GND	31	D6(+)	44	vd(-)
6	CTL2(-)	19	D0(+)	32	D6(-)	45	hd(+)
7	CTL3(+)	20	D0(-)	33	D7(+)	46	hd(-)
8	CTL3(-)	21	D1(+)	34	D7(-)	47	PCLK(+)
9	Cam_IO0	22	D1(-)	35	D8(+)	48	PCLK(-)
10	Cam_IO1	23	D2(+)	36	D8(-)	49	EXT_TRG(
							+)
11	Cam_IO2	24	D2(-)	37	D9(+)	50	EXT_TRG(
							-)
12	Cam_IO3	25	D3(+)	38	D9(-)		
13	Cam_IO4	26	D3(-)	39	D10(+)		

D0: LSB D11: MSB

VD: Vertical valid HD: Horizontal valid

PCLK: Dot clock

Remark1: Cam_IO0-7, CTL0-3 & EXT_TRG pin are only used for

customization (i.e. not used in standard product).

Remark2: The standard version is 10 bits compatible. Connect cable to D9-D0.

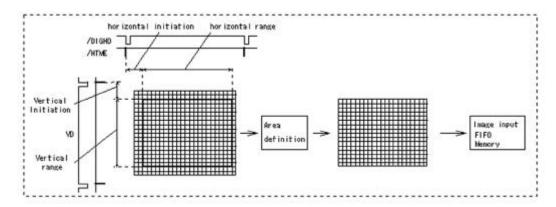
With the Viewer Software, 8 bits data of D9(MSB)-D2(LSB) are

displayed.

Please contact one of our sales rep. for 12 bits connection.

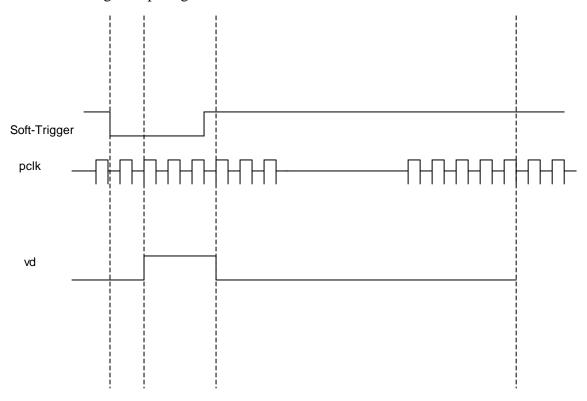
5. Image Signal

Image: Update 1 pixel by 1 clock



Size of board is $150 \text{mm} \times 100 \text{mm} \times 15 \text{mm}$.

6. Timing for capturing



Trigger from software. Wait for leading edge of "vd" at falling edge of "Soft-trigger". After detecting leading edge of "vd", image data transfer is prepared.

~ Transfer image for the amount of vertical pixels set.

Remark3: In external trigger mode, one transfer is automatically finalized when number of line is counted using "hd" signal, and effective line is transferred. (applies in customization) Remark4: Image data is latched by falling edge of pixel clock.

7. Connector

> C N 1 C N 3

CN1: LVDS input

Input LDVD signal from camera

Purpose-build cable for camera is required.

USB2 output CN3;

Connect USB2 cable to the PC.

LVDS-USB2.0 Converter Unit, Description of item

October 2002